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09/591,682	06/09/2000	Sheila M. Rader	CS-10246	3605

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EXAMINER	
THAI, XUAN MARIAN	

ART UNIT	PAPER NUMBER
2111	13

DATE MAILED: 02/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/591,682	Applicant(s) RADER ET AL.	
	Examiner XUAN M. THAI	Art Unit 2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5-16,20 and 31-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-16,20 and 31-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

RESPONSE TO AMENDMENT

1. This is in response to communications filed on October 22, 2003 and November 20, 2003. Claims 2-4,17-18, 17-28, 30 and 35-37 have been canceled. Claims 1, 5-16, 29 and 31-34 have been amended. Claims 1, 5-16, 29 and 31-34 remain pending in the instant application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1 and 5-7 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Chauvel et al. (USPN 6,321,299; Chauvel).

As per claims 1 and 12, Chauvel discloses the claimed invention including a data transfer system and method comprising: a plurality of peripheral interfaces [24a-c, 26a-c, interfaces 16, 20, 14b, SBUS interface; fig. 1]; a first memory [SDRAM 24 or Flash 26 or Cache 12a or 12b]; and a programmable direct memory access module [DMA controller 18] coupling the first memory to each of the plurality of peripheral interfaces [Fig. 1], wherein the programmable direct memory access module configures selectively programmable direct memory access channels between the first memory [SDRAM 24 or Flash 26 or Cache 12a or 12b] and respective ones of the plurality of peripheral interfaces [e.g. see fig. 1]; a first processor [processor 12] coupled to the programmable direct memory access module [DMA controller 18] and associated with the first memory [SDRAM 24 or Flash 26 or Cache 12a or 12b; see fig. 1] through a first shared bus (SBUS) connection coupling both the first processor and the first memory to the programmable memory access module [fig. 1]; a second memory [e.g. SDRAM 24 or Flash 26 or Cache 12a or 12b or DSP Cache (col. 2, lines 60)] coupled to the programmable direct memory access module [DMA controller 18], wherein the PDMA module configures the selectively DMA channels between the second memory and the respective ones of the plurality of peripheral interfaces [fig. 1]; and a second processor coupled to the PDMA module [DMA controller 18] and associated with the second memory [e.g. SDRAM 24 or Flash 26 or Cache 12a or 12b or DSP Cache (col. 2, lines 60)]; see fig. 1] through a second shared bus (e.g. DMA bus and DMA interface DATA and CTRL bus; fig. 1) that is independent of the first shared bus connection, coupling both the second processor (DSP) and the second memory (e.g. DSP Cache) to the programmable DMA module.

As per claim 5, further selectively programmable DMA data channels are configured between the first memory and the second memory is disclosed in Chauvel [col. 3, lines 17-60];

As per claim 6, wherein the DMA module [DMA controller 18] includes a programmable processor;

As per claim 7, wherein the PDMA module further includes a DMA controller 18 coupled to the programmable processor, wherein the processor configures the selectively programmable DMA channels between the first memory and the peripheral interfaces [col. 2, lines 65-67] via a dedicated DMA data transfer channel of the DMA.

4. Claims 1, 5-14, 29, and 31-34 are rejected under 35 U.S.C. 102(e) as being anticipated by Chauvel et al. (USPN 6,412,048; Chauvel).

As per claims 1 and 12, Chauvel discloses the claimed invention including a data transfer system and method comprising: a plurality of peripheral interfaces [24a-c, 26a-c, interfaces 16, 20, SBUS interface; interface 14b; fig. 2]; a first memory [SDRAM 24 or Flash 26 or Cache 12a or 12b]; and a programmable direct memory access module [DMA controller 18] coupling the first memory to each of the plurality of peripheral interfaces [Fig. 2], wherein the programmable direct memory access module configures selectively programmable direct memory access channels between the first memory [SDRAM 24 or Flash 26 or Cache 12a or 12b] and respective ones of the plurality of peripheral interfaces [e.g. see fig. 2; col. 5, lines 20-67]; a first processor [processor 12] coupled to the programmable direct memory access module [DMA controller 18] and associated with the first memory [SDRAM 24 or Flash 26 or Cache 12a or 12b; see fig. 2] through a first shared bus (SBUS) connection coupling both the first processor and the first

memory to the programmable memory access module [fig. 2]; a second memory [e.g. SDRAM 24 or Flash 26 or Cache 12a or 12b or DSP Cache (col. 4, lines 46-48)] coupled to the programmable direct memory access module [DMA controller 18], wherein the PDMA module configures the selectively DMA channels between the second memory and the respective ones of the plurality of peripheral interfaces [fig. 2; col. 5, lines 20-67]; and a second processor coupled to the PDMA module [DMA controller 18] and associated with the second memory [e.g SDRAM 24 or Flash 26 or Cache 12a or 12b or DSP Cache (col. 4, lines 46-48)]; see fig. 2] through a second shared bus (e.g. DMA bus and DMA interface DATA and CTRL bus; fig. 2) that is independent of the first shared bus connection, coupling both the second processor (DSP) and the second memory (e.g. DSP Cache) to the programmable DMA module.

As per claim 5, further selectively programmable DMA data channels are configured between the first memory and the second memory is disclosed in Chauvel [col. 5, lines 20-67];

As per claim 6, wherein the DMA module [DMA controller 18] includes a programmable processor [col. 5, lines 20-30; col. 6, lines 1-20; col. 14, lines 65-66; col. 17, lines 19-40];

As per claim 7, wherein the PDMA module further includes a DMA controller 18 coupled to the programmable processor (fig. 2), wherein the processor configures the selectively programmable DMA channels between the first memory and the peripheral interfaces [col. 5, lines 20-67 bridging col. 6, lines 1-20] via a dedicated DMA data transfer channel of the DMA.

As per claim 8, the DMA module further comprises a scheduler [priority handler] for prioritizing data transfers over the respective ones of the selectively programmable data channels [see col. 6, lines 1-20; col. 15, lines 10-67 to col. 17, lines 1-40];

As per claims 9 and 10, Chauvel discloses the claimed invention including a direct memory access system comprising: a DMA controller [18] establishing DMA data channel and including a first interface [e.g. 24a-c, 26a-c, interfaces 16, 20, SBUS interface; interface 14b; fig. 2] for coupling to a first memory [SDRAM 24 or Flash 26 or Cache 12a or 12b; see fig. 2]; a second interface [e.g. 24a-c, 26a-c, interfaces 16, 20, SBUS interface; interface 14b; fig. 2]; a third interface [e.g. 24a-c, 26a-c, interfaces 16, 20, SBUS interface; interface 14b; fig. 2] for coupling to a second memory; and a processor coupled to the DMA controller (18) and coupled to the second interface [e.g. 24a-c, 26a-c, interfaces 16, 20, SBUS interface; interface 14b; fig. 2] and the third interface, wherein the processor configures DMA data channel to transfer data between a programmable selectable respective one or more of the plurality of nodes and at least one of the first memory and the second memory [fig. 2; col. 5, lines 20-67];

As per claim 11, further comprises a scheduler [priority handler & state machine] for prioritizing data transfer via the DMA channel according to predetermined priorities [see col. 6, lines 1-20; col. 15, lines 10-67 to col. 17, lines 1-40];

As per claim 12, Chauvel discloses the method for performing DMA, the method comprising: receiving a request for DMA transfers [see col. 5, lines 20-67]; configuring code to establish a DMA data channel between a node and a DMA interface [see col. 5, lines 20-67]; transferring data between the node and the DMA interface along the direct memory access data channel [col. 5, lines 20-67];

As per claim 13, wherein the receiving step comprises receiving a timed request for a DMA transfer [see col. 17, lines 14-40];

As per claim 14, further comprising: prioritizing data [e.g. col. 15, lines 11-40; col. 17, lines 14-40].

As per claim 29, Chauvel discloses a processor communication system comprising: a first processor (12) DMA interface [e.g. DMA interface 16 or SBUS interface]; a second processor DMA interface (e.g. DMA interface 16); one or more peripheral ports [interfaces 14b or LCD controller interface 20]; a first data bus [e.g. SBUS]; a programmable controller [DMA Controller 18] comprising a plurality of registers [e.g. stack 18c or FIFO 18b] in communication with said first data bus for maintaining data communication, with the controller being operable for storing and retrieving data from the plurality of registers to establish multiple data transfers between said first processor interface and one or more peripheral ports [fig. 2, see col. 5, lines 20-67]; and a second data bus (e.g. DATA and CTL bus) couple to the programmable controller and said second processor DMA interface (e.g. DMA interface 16), wherein the programmable controller [DMA controller 18] is operable for establishing multiple data transfers between the second processor DMA interface via said second data bus, and at least one of said first processor DMA interface and said one or more peripheral ports (col. 5, lines 20-67).

As per claim 31, Chauvel discloses wherein the programmable processor prioritizes the multiple data transfers by storing and retrieving data from a plurality of registers [stacks or FIFO buffers; e.g. col. 15, lines 11-40; col. 17, lines 14-40].

As per claim 32, Chauvel discloses wherein a second processor interface comprising a DSP DMA interface [16];

As per claim 33, wherein the programmable controller is operable for establishing multiple virtual DMA channels [col. 5, lines 20-67];

As per claim 34, comprising embedded DMA memory for use with first processor [e.g. memory 12b or SDRAM].

5. Claims 1, 5-16, 29, and 31-34 are rejected under 35 U.S.C. 102(b) as being anticipated by Yokoyama et al. (USPN 5,678,060; Yokoyama).

As per claims 1 and 12, Yokoyama discloses the claimed invention including a data transfer system and method comprising: a plurality of peripheral interfaces [90B]; a first memory [5]; and a programmable direct memory access module [DMA controller 200] coupling the first memory to each of the plurality of peripheral interfaces [Fig. 1], wherein the programmable direct memory access module configures selectively programmable direct memory access channels between the first memory [5] and respective ones of the plurality of peripheral interfaces [90B]; a first processor [processor 4] coupled to the programmable direct memory access module [DMA controller module 50] and associated with the first memory [5] through a first shared bus (system bus 6) connection coupling both the first processor and the first memory to the programmable memory access module [fig. 1]; a second memory [e.g. 30] coupled to the programmable direct memory access module [DMA controller 200], wherein the PDMA module configures the selectively DMA channels between the second memory and the respective ones of the plurality of peripheral interfaces [col. 6, lines 20 et seq.]; and a second processor coupled to the PDMA module [DMA controller module 50] and associated with the second memory [e.g. memory 30]; see fig. 1] through a second shared bus (e.g. 80) that is independent of the first shared bus connection, coupling both the second processor (10) and the second memory (e.g. 30) to the programmable DMA module (see figs. 1 and 7; col. 6, lines 20 et seq.).

As per claim 5, further selectively programmable DMA data channels are configured between the first memory and the second memory is disclosed [col. 6, lines 20 et seq.];

As per claim 6, wherein the DMA module [DMA controller module] includes a programmable processor [e.g. processor 10];

As per claim 7, wherein the PDMA module further includes a DMA controller 200 coupled to the programmable processor (fig. 1), wherein the processor configures the selectively programmable DMA channels between the first memory and the peripheral interfaces via a dedicated DMA data transfer channel of the DMA (e.g. col. 6, lines 20 et seq).

As per claim 8, the DMA module further comprises a scheduler [arbiter] for prioritizing data transfers over the respective ones of the selectively programmable data channels [see col. 7, lines 30-35; col. 8, lines 6-9].

As per claims 9 and 10, Yokoyama discloses the claimed invention including a direct memory access system comprising: a DMA controller [200] establishing DMA data channel and including a first interface [90C] for coupling to a first memory [memory 5]; a second interface [e.g. 90A] for coupling a plurality of nodes; a third interface [600 or 201] for coupling to a second memory (memory 30); and a processor (10) coupled to the DMA controller (200) and coupled to the second interface [90A] and the third interface (600 or 201), wherein the processor configures DMA data channel to transfer data between a programmable selectable respective one or more of the plurality of nodes and at least one of the first memory and the second memory [fig. 1; col. 6 et seq]; the plurality of nodes including a plurality of peripheral interfaces (e.g. 500 and 90B).

As per claim 11, further comprises a scheduler [arbiter] for prioritizing data transfer via the DMA channel according to predetermined priorities [see col. 7, lines 30-35; col. 8, lines 6-9];

As per claim 13, wherein the receiving step comprises receiving a timed request for a DMA transfer [see col. 10, lines 18-67];

As per claim 14, further comprising: prioritizing data [e.g. see col. 7, lines 30-35; col. 8, lines 6-9].

As per claims 15 and 16, Yokoyama discloses the method of interrupting and resuming the transferring of data in the event a higher priority DMA data transfer is required [e.g. col. 7, lines 30-35].

As per claim 29, Yokoyama discloses a processor communication system comprising: a first processor (4) DMA interface [e.g. interface 70 or 90C]; a second processor (e.g. 10) DMA interface (e.g. 600 or 201); one or more peripheral ports [90A]; a first data bus [e.g. 6]; a programmable controller [DMA Controller 200] comprising a plurality of registers [e.g. 210, 215, 220, 225, 265, or 250] in communication with said first data bus for maintaining data communication, with the controller being operable for storing and retrieving data from the plurality of registers to establish multiple data transfers between said first processor interface and one or more peripheral ports [e.g. fig. 7]; and a second data bus (e.g. 80) couple to the programmable controller and said second processor DMA interface, wherein the programmable controller is operable for establishing multiple data transfers between the second processor DMA interface via said second data bus, and at least one of said first processor DMA interface and said one or more peripheral ports (figs. 1 and 7).

As per claim 32, Yokoyama discloses wherein a second processor interface comprising a DSP DMA interface [600];

As per claim 33, wherein the programmable controller is operable for establishing multiple virtual DMA channels [col. 4, lines 40-60];

As per claim 34, comprising embedded DMA memory for use with first processor [e.g. memory 5 or 40].

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chauvel et al. (USPN 6,412,048; Chauvel) in view of Kamiya (USPN 5,809,335).

As per claims 15 and 16, Heath discloses the claimed invention except for being silent on the method of interrupting and resuming the transferring of data in the event a higher priority DMA data transfer is required. Kamiya discloses that it is known at the time the invention was made to provide a capability in DMA data transfer to interrupt and resume the transfer of data through a channels such that the lower priority data transfer is interrupted so the higher priority data transfer can take place [see abstract]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the capabilities for interrupting and resuming the lower priority DMA data transfer as taught by Kamiya in the Chauvel system in that Kamiya states that by providing the apparatus with capability of carrying out interruption and resumption of DMA block transfer, important data that have urgent need can be efficiently transfer in an efficient and prompt manner [see col. 1, lines 5-12, and 44-48].

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

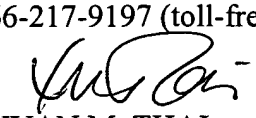
9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to XUAN M. THAI whose telephone number is 703-308-2064. The examiner can normally be reached on Monday to Friday from 8:30 A.M. to 5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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